

REMARKS/ARGUMENTS

Claims 1-16 and 19 remain in the application. Claims 17 and 18 were previously cancelled. Allowability of claims 3, 4, 6, 8, 11, 12, 14 and 16 is noted. Claim 6 is amended to correct informalities noted in the office action. Claims 3, 4, 6, 8, 11, 12, 14 and 16 are amended to place the claims in independent form as suggested in the Office action. Claims 1 and 9 are amended to further clarify the claims. No new matter is added by these amendments.

A. Rejections under 35 U.S.C. 102

Claims 1, 2, 9, 10, 17, 18 and 19 were rejected under 35 U.S.C. 102 based upon the Stamm reference. This rejection is respectfully traversed. Claim 1 calls for a system in which a cache transaction request is issued by one of the plurality of system components and addressed to the processor where the request indicates a request to perform a cache coherency operation. At least this feature of claim 1 is not shown or suggested in the relied on reference.

Table B in Stamm lists "cache coherency commands" that appear to be read and write commands that implicitly indicate that the CPU should perform a cache operation rather than an explicit command to perform a particular cache coherency operation. A read or write command is not properly defined as a cache transaction request. Stamm notes at column 7, lines 52-54, a cache coherency command will not necessarily cause a CPU to perform any cache operation. Claim 1 is further clarified to indicate that the cache transaction request is issued prior to a memory access request as taught in the specification at page 8, line 4 of the specification. The commands listed in Table B are not fairly construed as a cache transaction request as now called for in claim 1.

For at least these reasons claim 1 and claims 2 and 19 that depend from claim 1 are believed to be distinct with respect to the Stamm reference. Additionally, with respect to claim 19 the cited portion of Stamm (col. 4, lines 20-22) does not appear to show or suggest any of the specific limitations of claim 19.

Claim 9 calls for initiating a cache coherency transaction on the system bus using one of the plurality of modules other than the processing unit. Claim 9, as amended, clarifies that the module initiating the cache coherency transaction is not a processing unit. This amendment distinguishes claim 9 over Stamm, which the Office action asserts shows a second processor initiating a cache coherency transaction on a system bus. For at least this reason claim 9 and claim 10 that depends from claim 9 are believed to be allowable over Stamm.

B. Rejections under 35 U.S.C. 103.

Claims 5, 7, 13 and 15 were rejected under 35 U.S.C. 103 based upon the Stamm reference in view of Farrall. This rejection is respectfully traversed.

Claims 5 and 7 are distinct from Stamm for at least the reasons set out above with respect to claim 1. Claim 13 and 15 are distinct from Stamm for at least the reasons set out above with respect to claim 9. Farrall does not supply the deficiencies of Stamm.

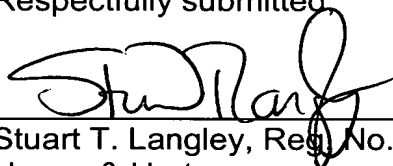
C. Conclusion.

In view of all of the above, the claims are now believed to be allowable and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is requested to contact Applicants' attorney at the telephone number listed below.

Eight additional independent claims are presented by this amendment bringing the total number of independent claims to 10. A check in the amount of \$1400 for the seven independent claims in excess of three previously paid for is enclosed herewith. Any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

April 27, 2005

Respectfully submitted



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